	L #	Hits	Search Text	DBs
1	L1	570	(renam$3 reorder$3) near20 pipelin$3	USPAT; US-PGPUB
2	L2	29331	(dependen$3 conflict$3) near10 (bit flag tag field)	USPAT; US-PGPUB
3	L3	1	1 near99 2	USPAT; US-PGPUB
4	L4	163	1 and 2	USPAT; US-PGPUB
5	L5	49	(renam$3 reorder$3) near20 pipelin$3	EPO; JPO; DERWENT; IBM_TDB
6	L6	4535	(dependen$3 conflict$3) near10 (bit flag tag field)	EPO; JPO; DERWENT; IBM_TDB
7	L7	2	5 and 6	EPO; JPO; DERWENT; IBM_TDB

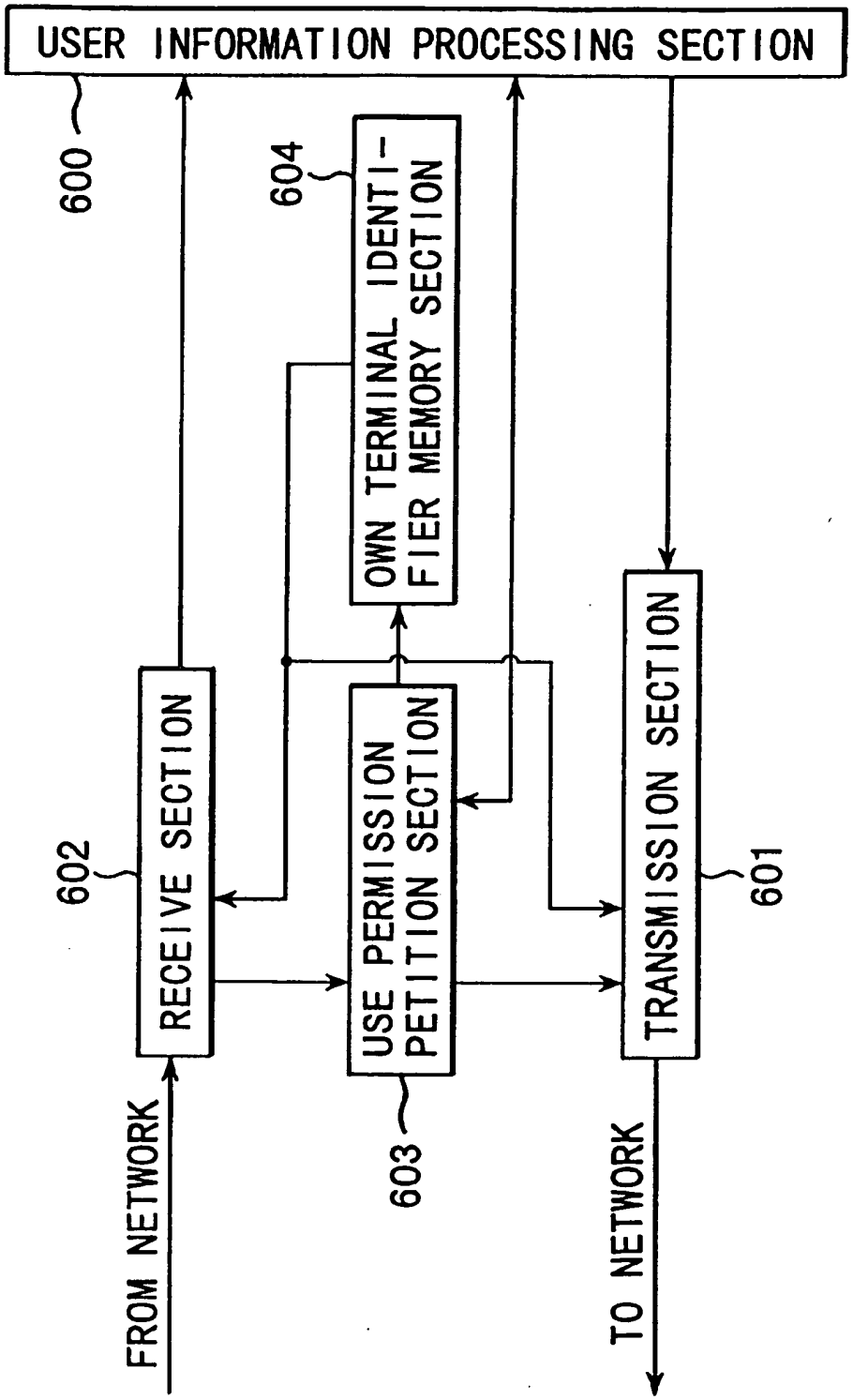

USER INFORMATION PROCESSING SECTION
600
604
OWN TERMINAL IDENTI-FIER MEMORY SECTION
602
RECEIVE SECTION
USE PERMISSION PETITION SECTION
603
TRANSMISSION SECTION
601
FROM NETWORK
TO NETWORK

FIG. 14

	Document ID	U	Title	Current OR
1	EP 709769 A	☐	Pipeline microprocessor capable of issuing and executing multiple instructions - performs source operand dependency analysis, register re=naming and provides rapid pipeline recovery for microprocessor issuing and executing multiple instructions out of order in single machine cycle	
2	EP 433864 A	☐	Hardware pipeline breaks minimiser - minimises hardware pipeline breaks using software scheduling techniques during compilation	

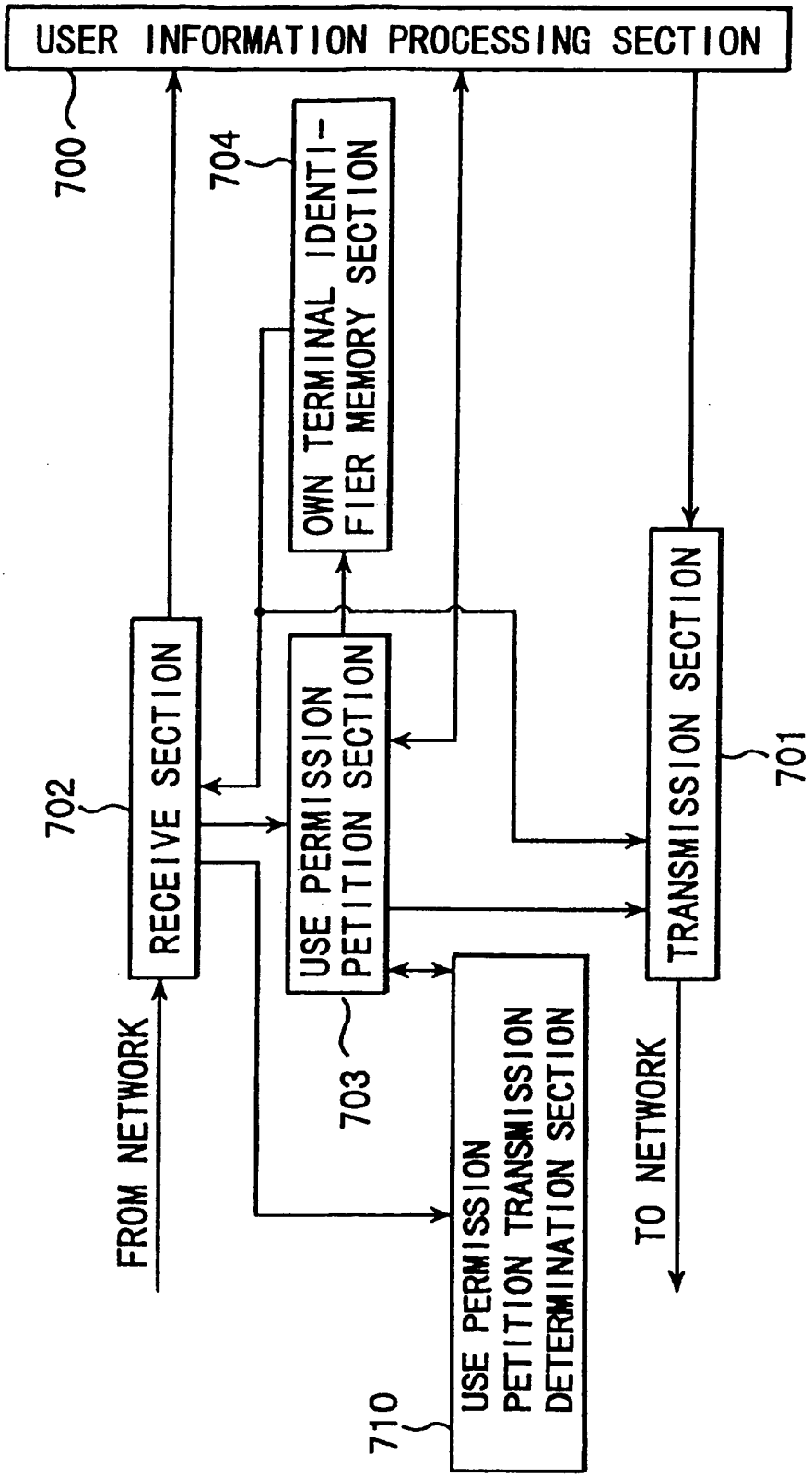

USER INFORMATION PROCESSING SECTION
700
704
OWN TERMINAL IDENTI-FIER MEMORY SECTION
RECEIVE SECTION
702
USE PERMISSION PETITION SECTION
703
TRANSMISSION SECTION
701
FROM NETWORK
TO NETWORK
USE PERMISSION PETITION TRANSMISSION DETERMINATION SECTION
710

FIG. 15

	Document ID	U	Title	Current OR
1	US 20030217249 A1	☐	Method and apparatus for virtual register renaming to implement an out-of-order processor	712/217
2	US 20030208672 A1	☒	Method and system for pipeline reduction	712/200
3	US 20030208665 A1	☒	Reducing data speculation penalty with early cache hit/miss prediction	711/169
4	US 20030182542 A1	☒	Method and apparatus for controlling execution of speculations in a processor based on monitoring power consumption	712/235
5	US 20030154364 A1	☒	MECHANISM FOR INSTRUCTION DATA FORWARDING IN A PIPELINE PROCESSOR	712/218
6	US 20030149865 A1	☒	Processor that eliminates mis-steering instruction fetch resulting from incorrect resolution of mis-speculated branch instructions	712/244
7	US 20030149862 A1	☒	Out-of-order processor that reduces mis-speculation using a replay scoreboard	712/217
8	US 20030135714 A1	☒	Method and apparatus for pre-processing instructions for a processor	712/217
9	US 20030126406 A1	☒	Stick and spoke replay	712/200
10	US 20030043665 A1	☒	LOW-POWER CIRCUIT STRUCTURES AND METHODS FOR CONTENT ADDRESSABLE MEMORIES AND RANDOM ACCESS MEMORIES	365/204
11	US 20030033511 A1	☒	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
12	US 20020194457 A1	☒	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
13	US 20020152259 A1	☒	Pre-committing instruction sequences	709/201
14	US 20020144098 A1	☒	Register rotation prediction and precomputation	712/221
15	US 20020129224 A1	☒	Method for handling 32 bit results for an out-of-order processor with A 64 bit architecture	712/209
16	US 20020083304 A1	☐	Rename finish conflict detection and recovery	712/218
17	US 20020083293 A1	☒	Register file circuitry	711/203

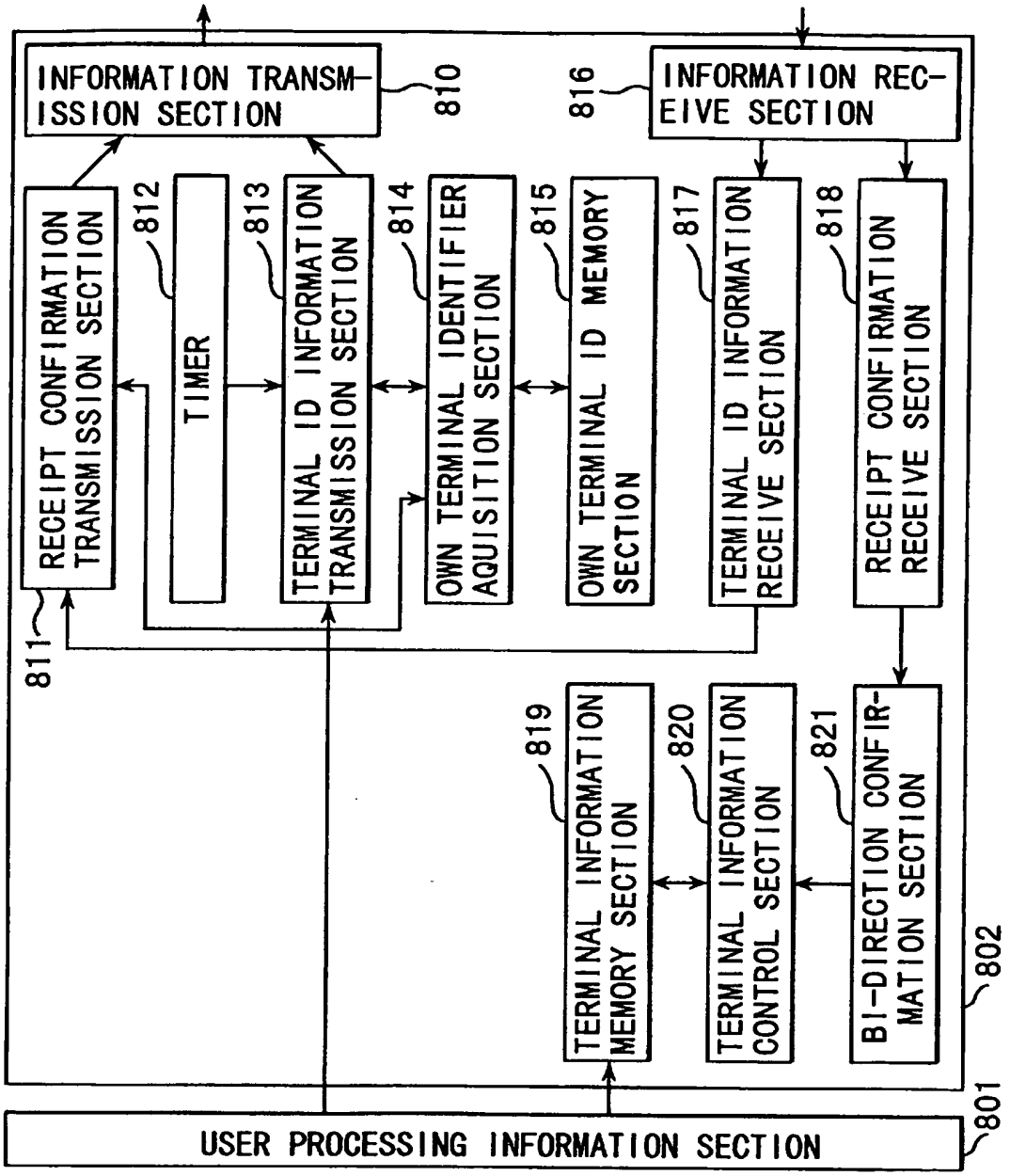
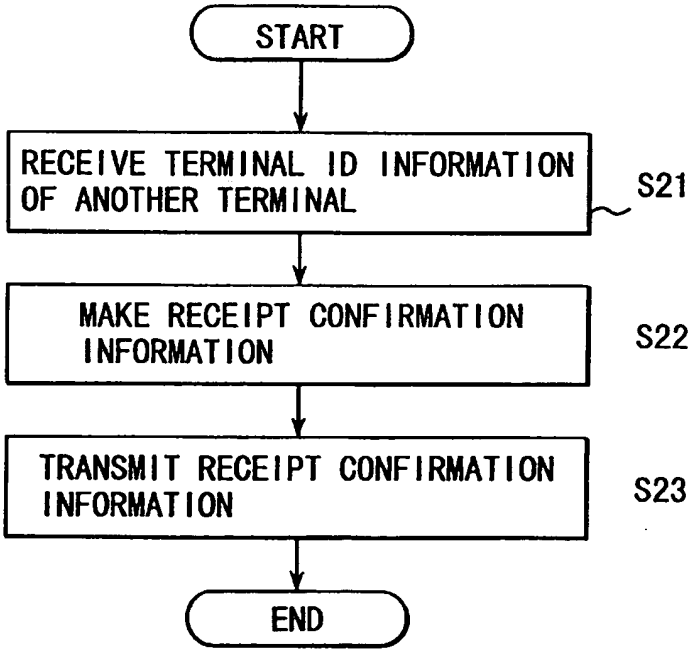

INFORMATION TRANSMISSION SECTION
810
816
INFORMATION RECEIVE SECTION
RECEIPT CONFIRMATION TRANSMISSION SECTION
811
812
TIMER
813
TERMINAL ID INFORMATION TRANSMISSION SECTION
814
OWN TERMINAL IDENTIFIER AQUISITION SECTION
815
OWN TERMINAL ID MEMORY SECTION
817
TERMINAL ID INFORMATION RECEIVE SECTION
818
RECEIPT CONFIRMATION RECEIVE SECTION
819
TERMINAL INFORMATION MEMORY SECTION
820
TERMINAL INFORMATION CONTROL SECTION
821
BI-DIRECTION CONFIRMATION SECTION
802
801
USER PROCESSING INFORMATION SECTION

FIG. 16

	Document ID	U	Title	Current OR
18	US 20020035677 A1	☒	METHOD AND APPARATUS FOR PRE-PROCESSING INSTRUCTIONS FOR A PROCESSOR	712/217
19	US 20020023204 A1	☒	Universal load address/value prediction scheme	712/239
20	US 20010054139 A1	☒	MECHANISM FOR POWER EFFICIENT PROCESSING IN A PIPELINE PROCESSOR	712/216
21	US 20010037434 A1	☒	Store to load forwarding using a dependency link file	711/146
22	US 20010014941 A1	☒	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
23	US 20010010069 A1	☒	Method for operating a non-blocking hierarchical cache throttle	711/122
24	US 6704855 B1	☒	Method and apparatus for reducing encoding needs and ports to shared resources in a processor	712/210
25	US 6697939 B1	☒	Basic block cache microprocessor with instruction history information	712/244
26	US 6684299 B2	☒	Method for operating a non-blocking hierarchical cache throttle	711/140
27	US 6633971 B2	☒	Mechanism for forward data in a processor pipeline using a single pipefile connected to the pipeline	712/218
28	US 6622225 B1	☒	System for minimizing memory bank conflicts in a computer system	711/158
29	US 6609190 B1	☒	Microprocessor with primary and secondary issue queue	712/214
30	US 6608771 B2	☒	Low-power circuit structures and methods for content addressable memories and random access memories	365/49
31	US 6604190 B1	☒	Data address prediction structure and a method for operating the same	712/207
32	US 6553482 B1	☒	Universal dependency vector/queue entry	712/216
33	US 6549990 B2	☒	Store to load forwarding using a dependency link file	711/146
34	US 6546453 B1	☒	Proprammable DRAM address mapping mechanism	711/5
35	US 6539471 B2	☒	Method and apparatus for pre-processing instructions for a processor	712/217
36	US 6523050 B1	☒	Integer to floating point conversion using one's complement with subsequent correction to eliminate two's complement in critical path	708/204
37	US 6499123 B1	☒	Method and apparatus for debugging an integrated circuit	714/724
38	US 6493820 B2	☒	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235

TERMINAL IDENTIFIER	UPDATING TIME
C1	11:00
C2	10:55
C3	11:01
C4	10:58

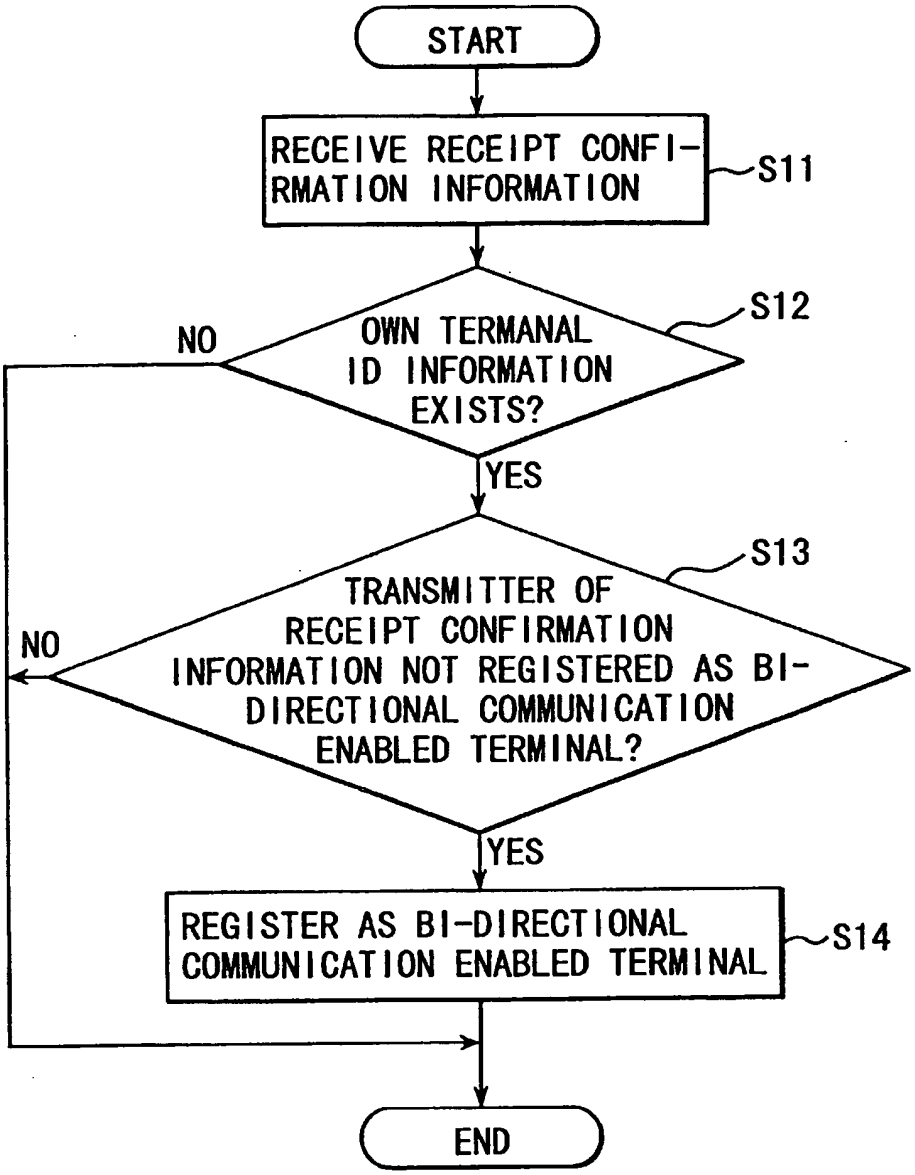
FIG. 17



[PROCESS TO BE PERFORMED WHEN TERMINAL ID INFORMATIN OF ANOTHER TERMINAL IS RECEIVED]

FIG. 19

	Document ID	U	Title	Current OR
39	US 6473837 B1	☒	Snoop resynchronization mechanism to preserve read ordering	711/146
40	US 6473832 B1	☒	Load/store unit having pre-cache and post-cache queues for low latency load memory operations	711/118
41	US 6463522 B1	☒	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
42	US 6427193 B1	☒	Deadlock avoidance using exponential backoff	711/146
43	US 6415360 B1	☒	Minimizing self-modifying code checks for uncacheable memory types	711/139
44	US 6393555 B1	☒	Rapid execution of FCMOV following FCOMI by storing comparison result in temporary register in floating point unit	712/222
45	US 6393549 B1	☒	Instruction alignment unit for routing variable byte-length instructions	712/204
46	US 6351803 B1	☒	Mechanism for power efficient processing in a pipeline processor	712/216
47	US 6339822 B1	☒	Using padded instructions in a block-oriented cache	712/213
48	US 6311261 B1	☒	Apparatus and method for improving superscalar processors	712/23
49	US 6308259 B1	☒	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
50	US 6282629 B1	☒	Pipelined processor for performing parallel instruction recording and register assigning	712/23
51	US 6275926 B1	☒	System and method for writing back multiple results over a single-result bus and processor employing the same	712/210
52	US 6269426 B1	☒	Method for operating a non-blocking hierarchical cache throttle	711/140
53	US 6266744 B1	☒	Store to load forwarding using a dependency link file	711/146
54	US 6260135 B1	☒	Parallel processing unit and instruction issuing system	712/214
55	US 6249862 B1	☒	Dependency table for reducing dependency checking hardware	712/218
56	US 6240509 B1	☒	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
57	US 6240502 B1	☒	Apparatus for dynamically reconfiguring a processor	712/15
58	US 6219823 B1	☒	Method and apparatus for moderating current demand in an integrated circuit processor	710/18
59	US 6217234 B1	☒	Apparatus and method for processing data with an arithmetic unit	709/247
60	US 6212629 B1	☒	Method and apparatus for executing string instructions	712/241
61	US 6212623 B1	☒	Universal dependency vector/queue entry	712/216



[PROCESS TO BE PERFORMED WHEN RECEIPT CONFIRMATION INFORMATION IS RECEIVED]

FIG. 18

	Document ID	U	Title	Current OR
62	US 6212622 B1	☒	Mechanism for load block on store address generation	712/216
63	US 6212602 B1	☒	Cache tag caching	711/122
64	US 6209084 B1	☒	Dependency table for reducing dependency checking hardware	712/233
65	US 6195744 B1	☒	Unified multi-function operation scheduler for out-of-order execution in a superscaler processor	712/215
66	US 6192462 B1	☒	Superscalar microprocessor including a load/store unit, decode units and a reorder buffer to detect dependencies between access to a stack cache and a data cache	712/23
67	US 6185675 B1	☒	Basic block oriented trace cache utilizing a basic block sequence buffer to indicate program order of cached basic blocks	712/238
68	US 6182210 B1	☒	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
69	US 6154815 A	☒	Non-blocking hierarchical cache throttle	711/140
70	US 6154812 A	☒	Method for inhibiting thrashing in a multi-level non-blocking cache system	711/122
71	US 6148371 A	☒	Multi-level non-blocking cache system with inhibiting thrashing	711/122
72	US 6141734 A	☒	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
73	US 6141421 A	☒	Method of asynchronous memory access	711/1
74	US 6122727 A	☒	Symmetrical instructions queue for high clock frequency scheduling	712/214
75	US 6119213 A	☒	Method for addressing data having variable data width using a fixed number of bits for address and width defining fields	711/202
76	US 6112019 A	☒	Distributed instruction queue	712/214
77	US 6108769 A	☒	Dependency table for reducing dependency checking hardware	712/216
78	US 6081873 A	☒	In-line bank conflict detection and resolution in a multi-ported non-blocking cache	711/131
79	US 6081656 A	☒	Method for deriving a double frequency microprocessor from an existing microprocessor	716/3
80	US 6058466 A	☒	System for allocation of execution resources amongst multiple executing processes	712/15
81	US 6052775 A	☒	Method for non-intrusive cache fills and handling of load misses	712/215
82	US 6047369 A	☒	Flag renaming and flag masks within register alias table	712/217
83	US 6035374 A	☒	Method of executing coded instructions in a multiprocessor having shared execution resources including active, nap, and sleep states in accordance with cache miss latency	711/118
84	US 6006326 A	☒	Apparatus for restraining over-eager load boosting in an out-of-order machine using a memory disambiguation buffer for determining dependencies	712/217

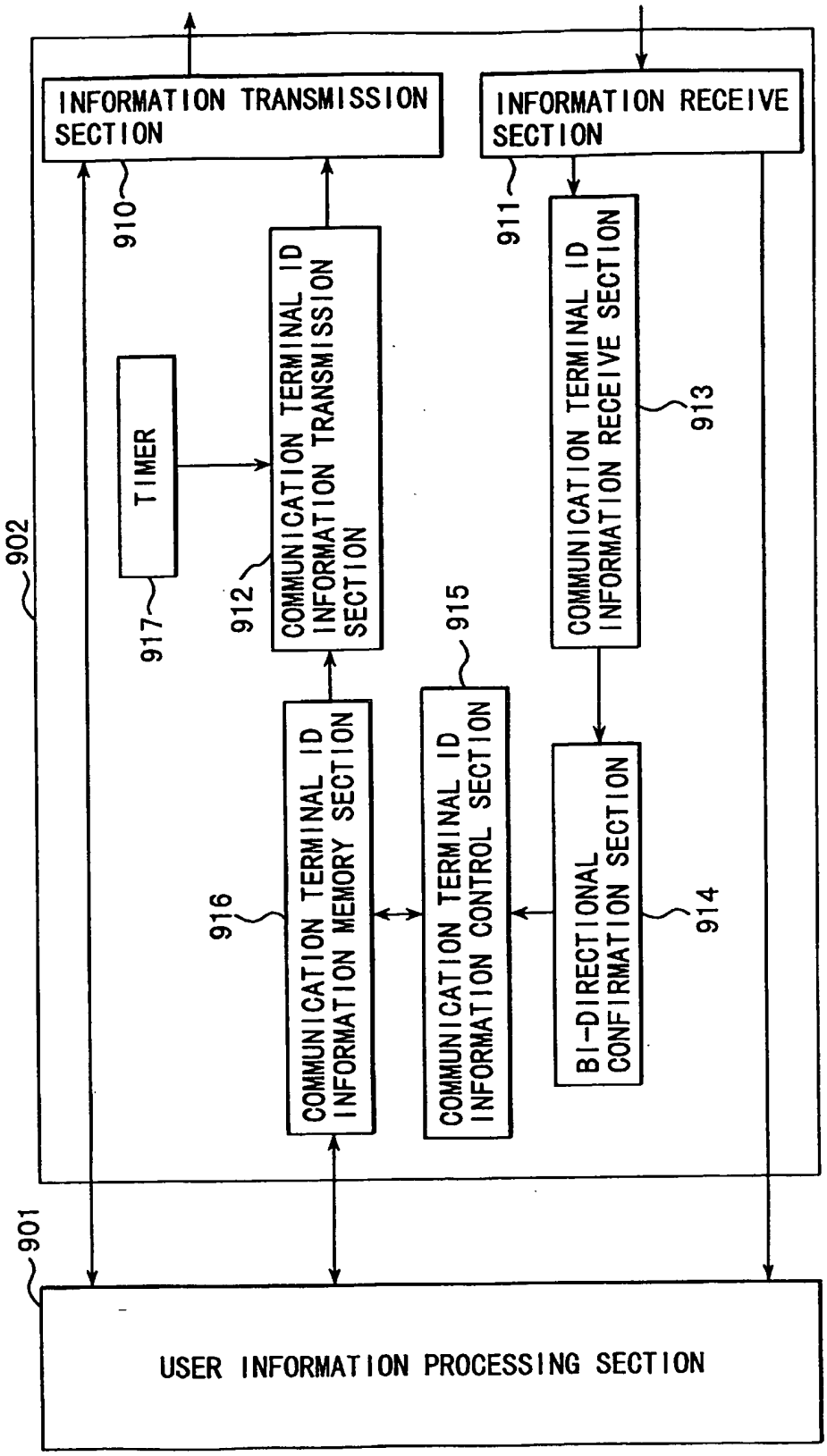

INFORMATION TRANSMISSION SECTION
910
INFORMATION RECEIVE SECTION
911
TIMER
917
COMMUNICATION TERMINAL ID INFORMATION TRANSMISSION SECTION
912
COMMUNICATION TERMINAL ID INFORMATION RECEIVE SECTION
913
902
915
COMMUNICATION TERMINAL ID INFORMATION MEMORY SECTION
916
COMMUNICATION TERMINAL ID INFORMATION CONTROL SECTION
BI-DIRECTIONAL CONFIRMATION SECTION
914
901
USER INFORMATION PROCESSING SECTION

FIG. 20

	Document ID	U	Title	Current OR
85	US 6006324 A	☒	High performance superscalar alignment unit	712/204
86	US 5999727 A	☒	Method for restraining over-eager load boosting using a dependency color indicator stored in cache with both the load and store instructions	712/225
87	US 5995727 A	☒	Video decompression	709/247
88	US 5987598 A	☒	Method and system for tracking instruction progress within a data processing system	712/227
89	US 5987594 A	☒	Apparatus for executing coded dependent instructions having variable latencies	712/216
90	US 5984512 A	☒	Method for storing video information	709/219
91	US 5983342 A	☒	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
92	US 5978864 A	☒	Method for thermal overload detection and prevention for an intergrated circuit processor	710/18
93	US 5974531 A	☒	Methods and systems of stack renaming for superscalar stack-based data processors	712/202
94	US 5974523 A	☒	Mechanism for efficiently overlapping multiple operand types in a microprocessor	712/23
95	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
96	US 5963154 A	☒	Technique for decoding variable and fixed length codes	341/67
97	US 5948106 A	☒	System for thermal overload detection and prevention for an integrated circuit processor	713/501
98	US 5930819 A	☒	Method for performing in-line bank conflict detection and resolution in a multi-ported non-blocking cache	711/131
99	US 5930491 A	☒	Identification of related instructions resulting from external to internal translation by use of common ID field for each group	712/209
100	US 5922069 A	☒	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
101	US 5898853 A	☒	Apparatus for enforcing true dependencies in an out-of-order processor	712/216
102	US 5890008 A	☒	Method for dynamically reconfiguring a processor	712/15
103	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
104	US 5884061 A	☒	Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle	712/217
105	US 5884059 A	☒	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
106	US 5878273 A	☒	System for microprogrammable state machine in video parser disabling portion of processing stages responsive to sequence.sub.-- end token generating by token generator responsive to received data	710/5

OWN TERMINAL IDENTIFIER	LIST OF RECEIPT ENABLED TERMINAL	LIST OF BI-DIRECTIONAL COMMUNICATION ENABLED TERMINALS

FIG. 21

TERMINAL IDENTIFIER	STATE OF COMMUNICATION	PERIPHERAL TERMINAL INFORMATION			UPDATING TIME
C1	BI-DIRECTION	C2	C4	C8	11:00
C2	BI-DIRECTION	C1	C3	C8	10:55
C3	BI-DIRECTION	C2	C4		11:01
C4	RECEIPT	C1	C3	C5	10:58

FIG. 22

	Document ID	U	Title	Current OR
107	US 5870580 A	☒	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
108	US 5850533 A	☒	Method for enforcing true dependencies in an out-of-order processor	712/216
109	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
110	US 5848287 A	☒	Superscalar microprocessor including a reorder buffer which detects dependencies between accesses to a pair of caches	712/23
111	US 5835792 A	☒	Token-based adaptive video processing arrangement	710/68
112	US 5835745 A	☒	Hardware instruction scheduler for short execution unit latencies	712/215
113	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
114	US 5832249 A	☒	High performance superscalar alignment unit	712/204
115	US 5829007 A	☒	Technique for implementing a swing buffer in a memory array	711/5
116	US 5828907 A	☒	Token-based adaptive video processing arrangement	710/68
117	US 5828886 A	☒	Compiling apparatus and method for promoting an optimization effect of a program	717/159
118	US 5828874 A	☒	Past-history filtered branch prediction	712/240
119	US 5826089 A	☒	Instruction translation unit configured to translate from a first instruction set to a second instruction set	717/146
120	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
121	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
122	US 5821885 A	☒	Video decompression	341/67
123	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
124	US 5819057 A	☒	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
125	US 5813033 A	☒	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
126	US 5805876 A	☒	Method and system for reducing average branch resolution time and effective misprediction penalty in a processor	712/234
127	US 5805853 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
128	US 5801973 A	☒	Video decompression	708/203
129	US 5798719 A	☒	Parallel Huffman decoder	341/67

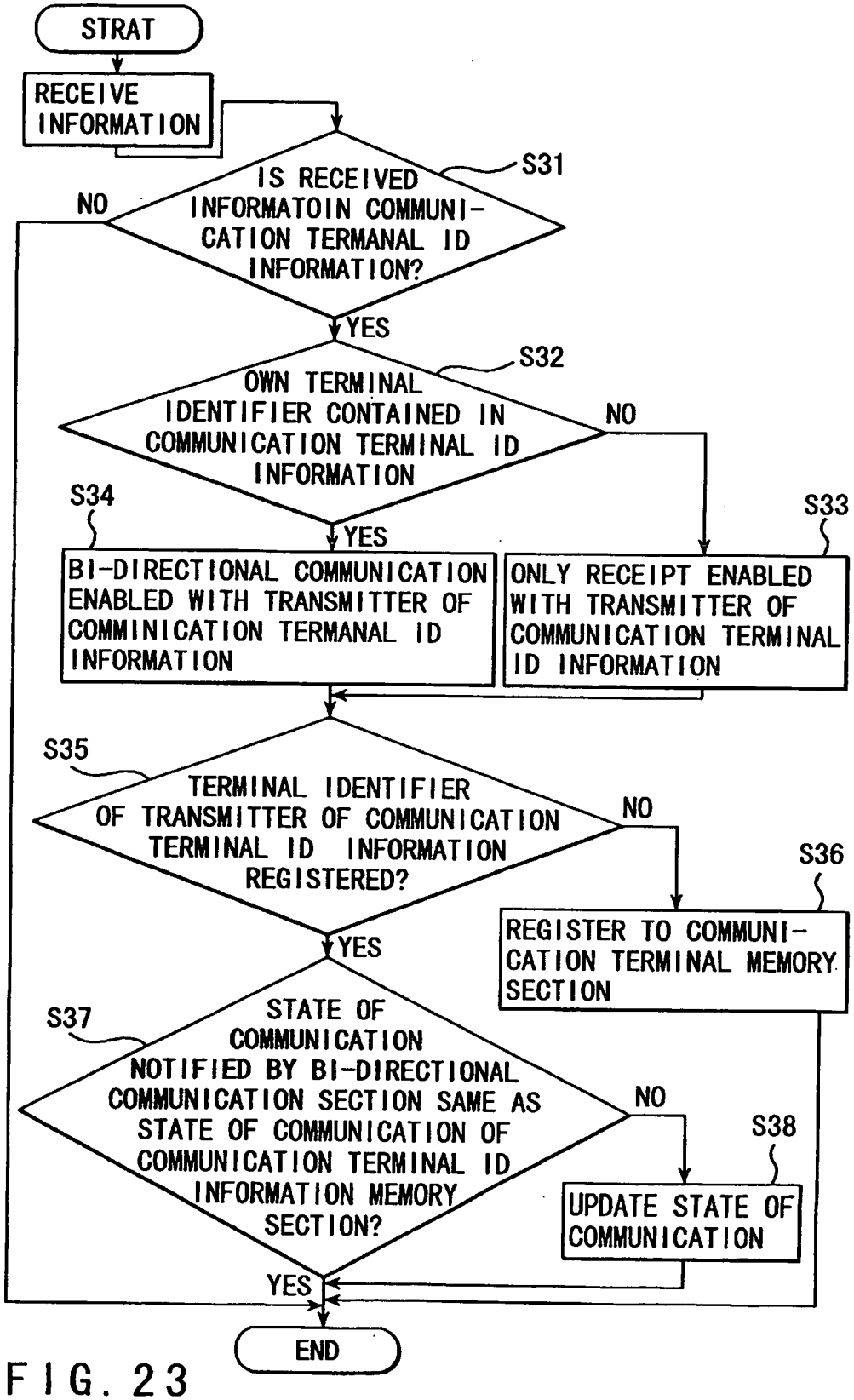

STRAT
RECEIVE INFORMATION
S31
IS RECEIVED INFORMATOIN COMMUNI-CATION TERMANAL ID INFORMATION?
NO
YES
S32
OWN TERMINAL IDENTIFIER CONTAINED IN COMMUNICATION TERMINAL ID INFORMATION
NO
YES
S34
BI-DIRECTIONAL COMMUNICATION ENABLED WITH TRANSMITTER OF COMMINICATION TERMANAL ID INFORMATION
S33
ONLY RECEIPT ENABLED WITH TRANSMITTER OF COMMUNICATION TERMINAL ID INFORMATION
S35
TERMINAL IDENTIFIER OF TRANSMITTER OF COMMUNICATION TERMINAL ID INFORMATION REGISTERED?
NO
YES
S36
REGISTER TO COMMUNI-CATION TERMINAL MEMORY SECTION
S37
STATE OF COMMUNICATION NOTIFIED BY BI-DIRECTIONAL COMMUNICATION SECTION SAME AS STATE OF COMMUNICATION OF COMMUNICATION TERMINAL ID INFORMATION MEMORY SECTION?
NO
YES
S38
UPDATE STATE OF COMMUNICATION
END

FIG. 23

	Document ID	U	Title	Current OR
130	US 5787474 A	☒	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
131	US 5781753 A	☒	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
132	US 5778245 A	☒	Method and apparatus for dynamic allocation of multiple buffers in a processor	712/23
133	US 5768629 A	☒	Token-based adaptive video processing arrangement	710/68
134	US 5768610 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
135	US 5768575 A	☒	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
136	US 5765035 A	☒	Recorder buffer capable of detecting dependencies between accesses to a pair of caches	712/216
137	US 5764946 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
138	US 5740460 A	☒	Arrangement for processing packetized data	348/473
139	US 5737629 A	☒	Dependency checking and forwarding of variable width operands	712/23
140	US 5727177 A	☒	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
141	US 5721855 A	☒	Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer	712/218
142	US 5717394 A	☒	Method and apparatus for encoding and decoding data	341/51
143	US 5703793 A	☒	Video decompression	382/232
144	US 5666506 A	☒	Apparatus to dynamically control the out-of-order execution of load/store instructions in a processor capable of dispatchng, issuing and executing multiple instructions in a single processor cycle	712/216
145	US 5649225 A	☒	Resynchronization of a superscalar processor	712/23
146	US 5634026 A	☒	Source identifier for result forwarding	712/217
147	US 5632023 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
148	US 5630149 A	☒	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
149	US 5625789 A	☒	Apparatus for source operand dependendency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle	712/217

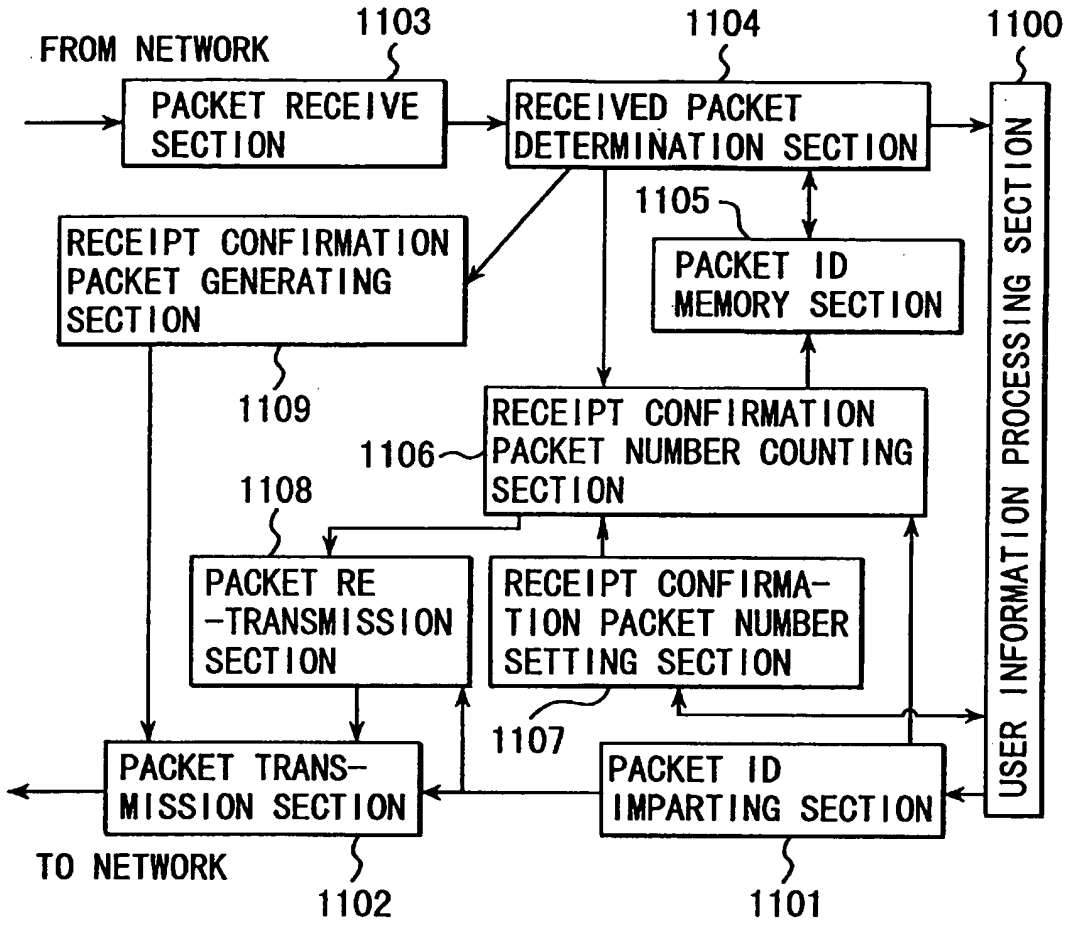

FROM NETWORK
1103
PACKET RECEIVE SECTION
1104
RECEIVED PACKET DETERMINATION SECTION
1100
USER INFORMATION PROCESSING SECTION
1105
PACKET ID MEMORY SECTION
RECEIPT CONFIRMATION PACKET GENERATING SECTION
1109
1106
RECEIPT CONFIRMATION PACKET NUMBER COUNTING SECTION
1108
PACKET RE-TRANSMISSION SECTION
RECEIPT CONFIRMATION PACKET NUMBER SETTING SECTION
1107
PACKET TRANSMISSION SECTION
PACKET ID IMPARTING SECTION
TO NETWORK
1102
1101

FIG. 24

	Document ID	U	Title	Current OR
150	US 5619662 A	☒	Memory reference tagging	712/216
151	US 5615350 A	☒	Apparatus to dynamically control the out-of-order execution of load-store instructions in a processor capable of dispatching, issuing and executing multiple instructions in a single processor cycle	712/218
152	US 5590352 A	☒	Dependency checking and forwarding of variable width operands	712/23
153	US 5586278 A	☒	Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor	712/235
154	US 5581719 A	☒	Multiple block line prediction	712/207
155	US 5564118 A	☒	Past-history filtered branch prediction	712/240
156	US 5546597 A	☒	Ready selection of data dependent instructions using multi-cycle cams in a processor performing out-of-order instruction execution	712/23
157	US 5519841 A	☒	Multi instruction register mapper	711/202
158	US 5471593 A	☒	Computer processor with an efficient means of executing many instructions simultaneously	712/235
159	US 5471207 A	☒	Compression of palettized images and binarization for bitwise coding of M-ary alphabets therefor	341/107
160	US 5404470 A	☒	Information processing apparatus for processing instructions by out-of-order execution	712/217
161	US 5150469 A	☒	System and method for processor pipeline control by selective signal deassertion	712/244
162	US 5119495 A	☒	Minimizing hardware pipeline breaks using software scheduling techniques during compilation	717/153
163	US 4965724 A	☐	Compiler system using reordering of microoperations to eliminate interlocked instructions for pipelined processing of assembler source program	717/160

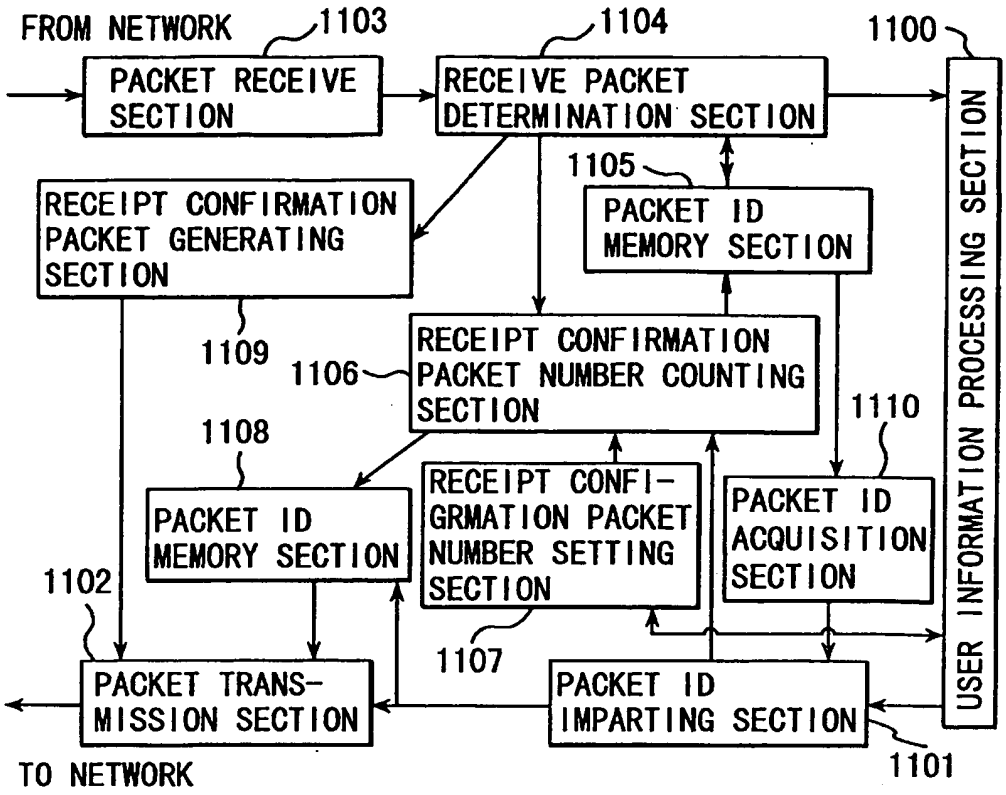

FROM NETWORK
1103
PACKET RECEIVE SECTION
1104
RECEIVE PACKET DETERMINATION SECTION
1100
USER INFORMATION PROCESSING SECTION
1105
PACKET ID MEMORY SECTION
RECEIPT CONFIRMATION PACKET GENERATING SECTION
1109
1106
RECEIPT CONFIRMATION PACKET NUMBER COUNTING SECTION
1110
1108
PACKET ID MEMORY SECTION
RECEIPT CONFI-GRMATION PACKET NUMBER SETTING SECTION
PACKET ID ACQUISITION SECTION
1102
1107
PACKET TRANS-MISSION SECTION
PACKET ID IMPARTING SECTION
1101
TO NETWORK

FIG. 25

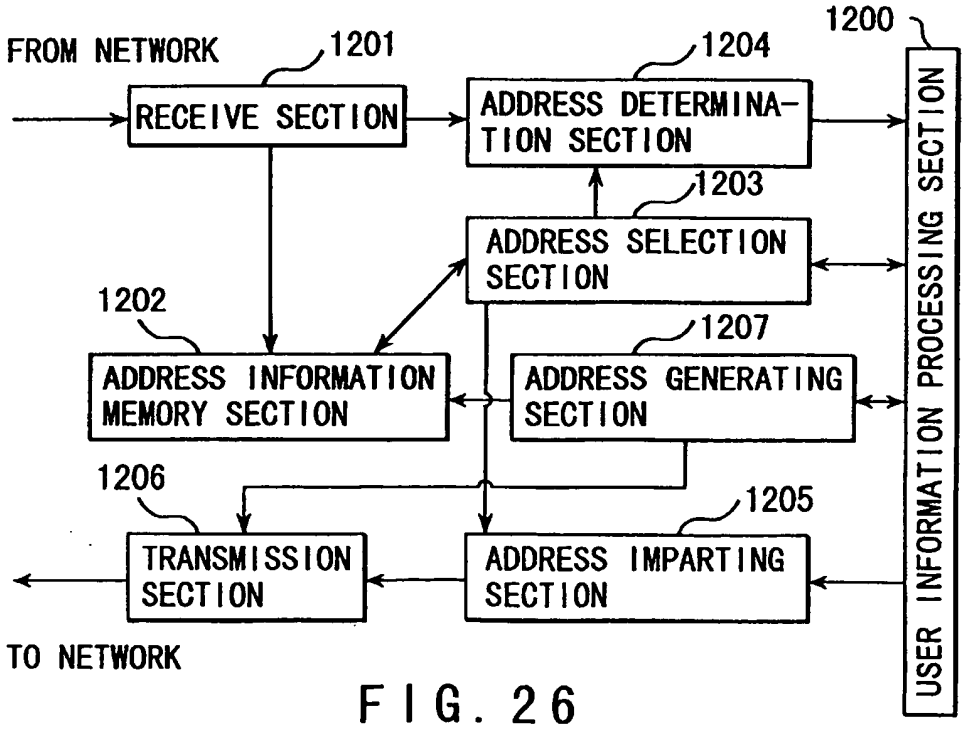

1200
FROM NETWORK
1201
RECEIVE SECTION
1204
ADDRESS DETERMINA-TION SECTION
1203
ADDRESS SELECTION SECTION
1202
1207
ADDRESS INFORMATION MEMORY SECTION
ADDRESS GENERATING SECTION
1206
1205
TRANSMISSION SECTION
ADDRESS IMPARTING SECTION
USER INFORMATION PROCESSING SECTION
TO NETWORK

FIG. 26